PURDUE MATERIALS ENGINEERING

Investigation of Microstructure Evolution in 3D Memory Devices

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Small solder micro-bumps are used to bond logic layers into a three-dimensional memory chip. These layers contain through-silicon-vias (TSVs) that transfer information through the chips. These 3D-stacked memory chips were cycled under various conditions in order to track intermetallic compound (IMC) growth, and morphological changes of the micro-bumps between the TSVs. The intermetallic growth rate correlates with t_{eff}, or time above 70% of the melting temperature of the solder. The IMC growth was not dependent on the placement of the bump within the 3D chip, although the layer of the bump did affect their height. Based on the data collected, when held at 85°C the micro-bumps will be 100% IMC in 7 years and 9 months.

JUNIPER NETWORKS

This work is sponsored by Juniper Networks, Sunnyvale, CA

Project Background

Problem Statement

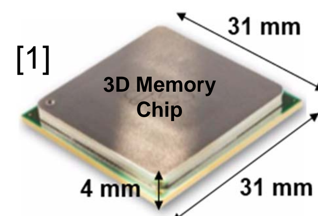
Juniper is concerned with the reliability of certain high risk components. This project set out to see how reliable these components are over time.

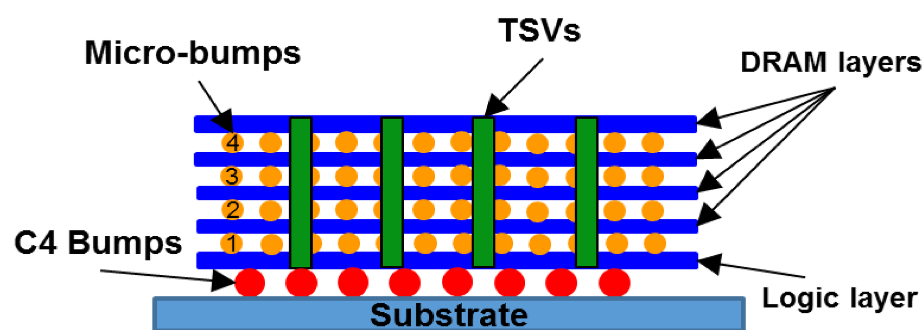
Goal

Estimate the long term reliability of 3D memory devices through accelerated testing, and to quantify microstructural changes of micro-bumps

3D-Stacked Memory Architecture

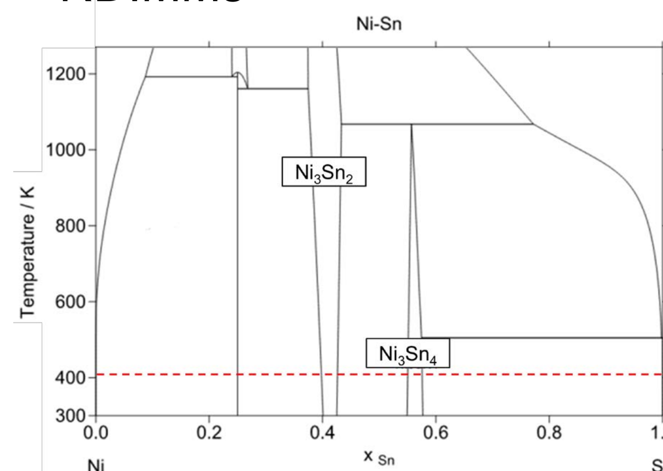
Three-dimensional (3D) memory devices utilize through-silicon-vias (TSVs) and micro-solder bumps to connect DRAM cells. The bumps in between each DRAM layer are identified as layer 1, 2, 3 or 4.





3D-Stacked Memory Performance

- Provides 15X the bandwidth of a DDR3 module
- Uses 70% less energy per bit than DDR3-1333
- Reduces latency due to massive parallelism
- Reduces footprint by 90% compared to current RDIMMs



As seen in the Ni-Sn system [2], the primary intermetallic is Ni_3Sn_4 and the secondary intermetallic is Ni_3Sn_2. at 423K (150°C)

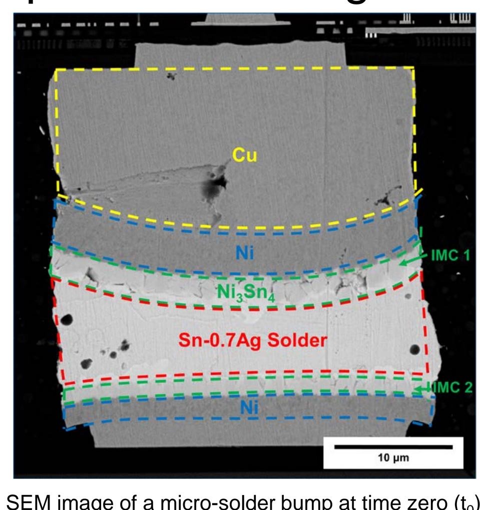
Experimental Procedure

Accelerated Testing

1. High Temperature Storage: Annealed at 150°C
2. Thermal Cycling: Cycled from -37°C to 101°C
3. Sequential Testing: Alternating HTS and TC

Measuring Intermetallic Compound (IMC)

Backscattered Scanning Electron (BSE) microscopy and Energy Dispersive X-ray Spectroscopy (EDS) were used to identify phases of IMC formed at the Ni and Sn interfaces. Using quantitative image analysis, the average IMC thickness was measured using the area of the IMC layer and the length of the layer.



SEM image of a micro-solder bump at time zero (t_0)

$$IMC\ thickness = \frac{Area\ of\ IMC\ layer}{Length}$$

Ni_3Sn_4 — Ni — Area — Length

70% of Melting Temperature

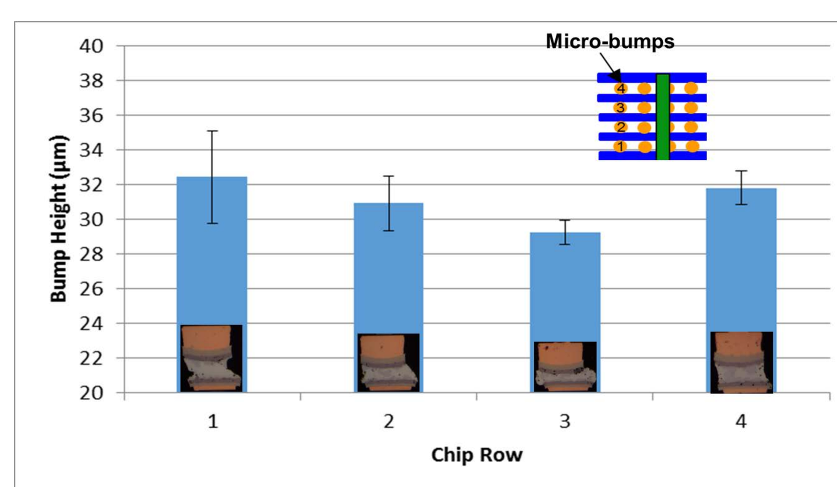
Intermetallic growth was tracked as a function of the amount of time that chips spent over a homologous temperature of 0.7 (T_h = 80°C). The cycled chips spent 26 minutes above this temperature for every two hour cycle, which is the effective time (t_{eff})

Results and Discussion

ANOVA Analysis of Position Dependency

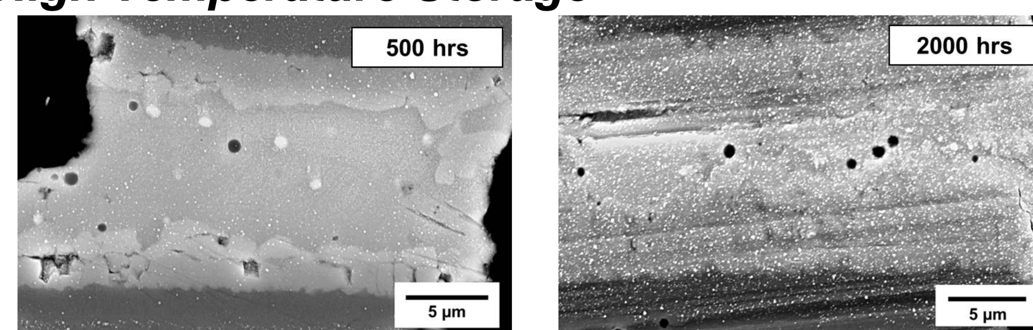
Data was analyzed to determine if the position of the micro-bumps within the chip affected their IMC growth or height. The model was analyzed with a standard alpha level of 0.05.

- The P-values for IMC dependence on chip layer were 0.51, 0.77, and 0.54 for the tree tests which indicates no dependence on chip layer for IMC growth.
- The P-values for IMC growth dependence on inner vs outer row were 0.22, 0.80, and 0.73 for the three tests which indicates that there is no dependence on inner or outer rows for IMC growth.
- The P-Value for height dependence on chip layer is 0.001, indicating a strong relationship between the chip layer and bump height. This relationship can be seen in the graph below.



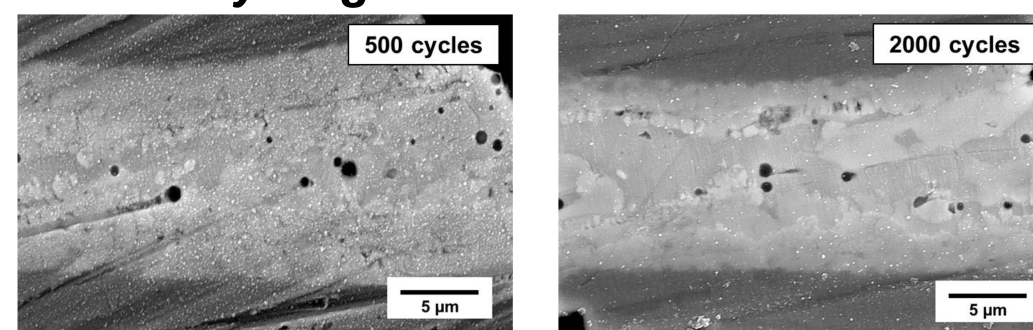
Bump height vs chip layer with representative bump images from sequential testing

High Temperature Storage



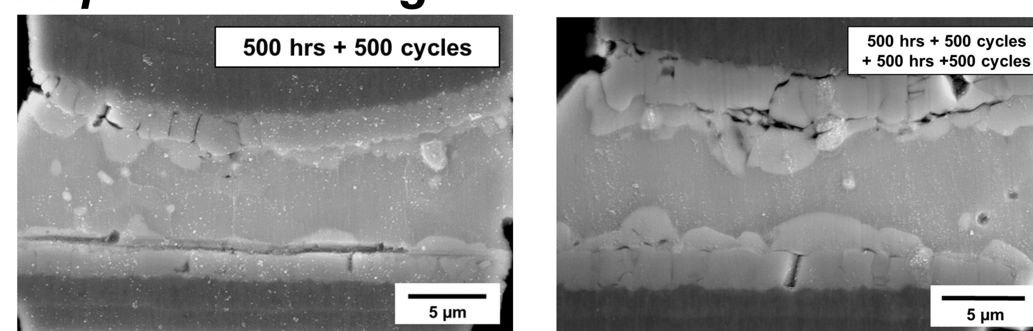
Rapid IMC growth, minimal grain boundaries and micro-cracks

Thermal Cycling



Largely increased grain size, increased IMC layer, minimal micro-cracks

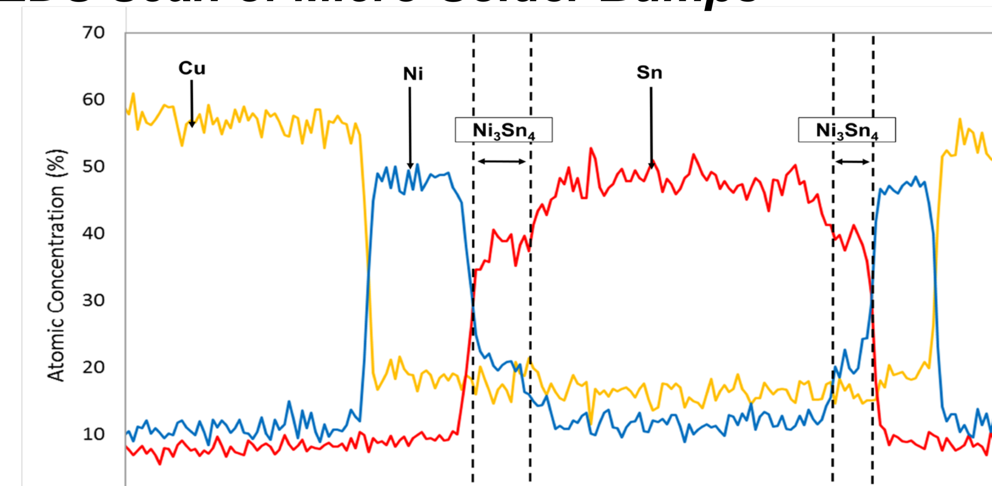
Sequential Testing



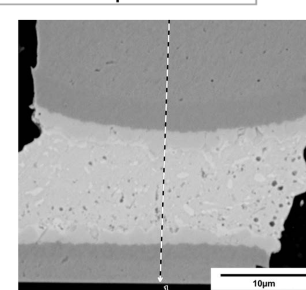
Slow IMC growth, larger grain boundaries and an increase in number of micro-cracks with time

Note: Pores within the solder are not identified as voids, but under-fill from surrounding matrix

EDS Scan of Micro-Solder Bumps



- EDS scan confirms Ni_3Sn_4 IMC presence in the chips
- IMC composition determined from atomic concentrations



Line scan location of micro-solder bump

Modified Arrhenius Analysis

IMC thickness can be estimated at any temperature using a modified Arrhenius equation:

$$x = x_o + At^n e^{\left(\frac{-Q}{RT}\right)}$$

x = final IMC thickness (µm)

x_o= initial IMC thickness after reflow (µm)

n = time exponent (0.46) [3]

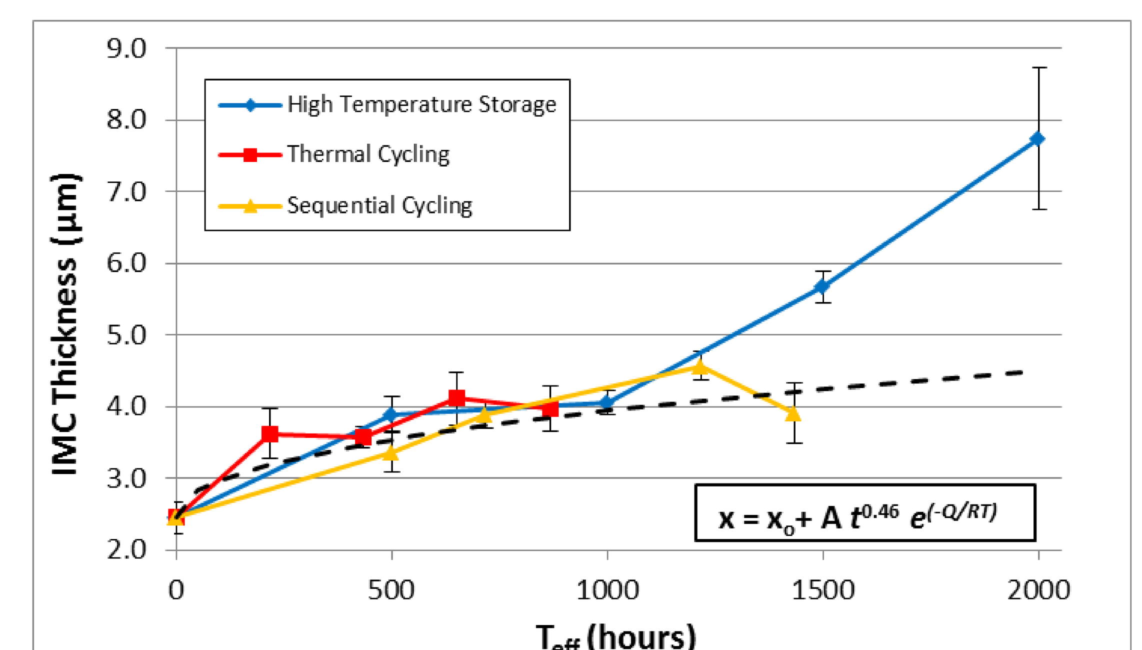
Q = Apparent activation energy of IMC (-41.7 $\frac{kJ}{mol}$) [3]

A = pre exponential factor ($\frac{\mu m}{s^n}$)

t = time (s)

T = Temperature (K)

- Time exponents on the order of 0.5 indicate a diffusion controlled growth mechanism
- The deviance of n from 0.5 accounts for the diffusion rate of Ni in Sn [3]
- Growth rate averages 1.4 nm/hr for Sequential testing and Thermal Cycling
- Growth rate is doubled with HTS at 3.2 nm/hr
- Growth estimate from Arrhenius equation at 85°C, which is standard server operating temperature, estimates that the micro bumps will be 100% IMC in 68,000 hours, or 7 years and 9 months



IM thickness versus T_{eff} fit with the Arrhenius equation (dashed)

Recommendations

High levels of intermetallic growth are unfavorable in the functional portions of solder joints because the increase in electrical resistivity in the intermetallic can lead to signal attenuation in the chip [4] and ultimately electronic or physical failure. At a standard operating temperature of 85°C, the micro-bumps in these chips are projected to be completely IMC in 7 years and 9 months.

It was also found that the placement of the micro-bump within the chip has no effect on how the micro-bump behaves under accelerated testing conditions.

Further testing should be done to determine the brittleness of these IMCs under high usage loads in order to determine whether physical degradation could cause failure before signal attenuation. We do not observe significant reliability risk for this 3D component based on our data including IMC growth rate, grain growth and micro-crack formation rate in the micro-bumps.

References

[1] Single Package HMC. Digital Image. Solid State Technology. Web.

[2] Ni-Sn Phase Diagram. Digital Image. National Physical Laboratory. Web.

[3] Xu, L. (2005). Isothermal and Thermal Cycling Aging on IMC Growth Rate in Lead-Free and Lead-Based Solder Interface. IEEE Transactions on Components and Packaging Technologies IEEE Trans. Comp. Package. Technol., 28(3), 408-414.

[4] Fields, R. (1991). Physical and Mechanical properties of Intermetallic Compounds Commonly Found in Solder Joints. Proceedings of TMS Symposium.